CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller including:

a memory built-in self-test engine capable of executing a memory built-in self-test; and

a memory built-in self-test signature generated on execution of the memory built-in self-test.

2. The built-in self-test controller of claim 1, wherein the memory built-in self-test signature register includes the results of at least one paranoid check.

3. The built-in self-test controller of claim 1, wherein the memory built-in self-test signature includes a bit indicating whether the memory built-in self-test is done.

4. The built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

5. The built-in self-test controller of claim 4, wherein the memory built-in self-test state machine comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state upon completing a flush of a plurality of memory components to a known state; and

a done state entered into upon completing the test of each of the memory components in the memory built-in self-test.

6. The built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

7. The built-in self-test controller of claim 6, wherein each of the memory built-in self-test engines comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

8. The built-in self-test controller of claim 1, further comprising:

a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test.

9. A built-in self-test controller including:

means for executing a memory built-in self-test; and

means for storing the results generated on execution of the memory executing means.

10. The built-in self-test controller of claim 9, wherein the memory storing means includes the results of at least one paranoid check.

11. The built-in self-test controller of claim 9, wherein the memory storing means includes a bit indicating whether the memory built-in self-test is done.

12. The built-in self-test controller of claim 9, wherein the memory executing means comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

13. The built-in self-test controller of claim 9, wherein the memory executing means comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

14. The built-in self-test controller of claim 9, further comprising:

means for executing a logic built-in self-test and storing the results thereof; and

means for storing the results of an executed logic built-in self-test.

15. A integrated circuit device including:

a plurality of memory components;

a testing interface; and

a built-in self-test controller controlled through the testing interface, the built-in self-test controller including:

a memory built-in self-test engine capable of performing a memory built-in self-test; and

a memory built-in self-test signature generated upon an execution of the memory built-in self-test.

16. The integrated circuit device of claim 15, wherein the memory built-in self-test signature register is further capable of storing the results of at least one paranoid check.

17. The integrated circuit device of claim 15, wherein the memory built-in self-test signature register includes a bit indicating whether the memory built-in self-test is done.

18. The integrated circuit device of claim 15, wherein the memory built-in self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

19. The integrated circuit device of claim 15, wherein ~~the memory built-in self-test state machine~~ comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

a test state entered into from the flush state; and

a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

20. The integrated circuit device of claim 15, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

21. The integrated circuit device of claim 15, wherein the memory components include a static random access memory device.

22. The integrated circuit device of claim 15, wherein the testing interface comprises a Joint Test Action Group tap controller.

23. The integrated circuit device of claim 15, further comprising:

a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test.

24. A method for performing a memory built-in self-test, the method comprising:

externally resetting a memory built-in self-test engine and a memory built-in self-test signature;

generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine; and

reading the generated memory built-in self-test signature.

25. The method of claim 24, wherein the execution of the memory built-in self-test includes:

initiating a plurality of components and signals in a memory built-in self-test engine and the memory built-in self-test signature upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals; and

testing the flushed memory components.

26. The method of claim 25, wherein generating the memory built-in self-test signature includes:

storing the results of the testing in a memory built-in self-test signature register.

27. The method of claim 24, wherein generating the memory built-in self-test signature includes storing the results of the testing in a memory built-in self-testing register.

28. The method of claim 24, wherein performing the memory built-in self-test further includes at least one of:

performing at least one paranoid check; and

storing the results of the paranoid check in the memory built-in self-test signature register.

29. The method of claim 24, wherein performing the memory built-in self-test further includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done.

30. The method of claim 24, wherein externally resetting the memory built-in self-test engine includes externally resetting a memory built-in self-test engine including:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine.

31. The method of claim 30, wherein externally resetting the memory built-in self-test state machine includes externally resetting one of a plurality of memory built-in self-test state machines.

32. The method of claim 30, wherein flushing the contents of the memory components includes flushing the contents of a plurality of static random access memories.

33. A method for performing a built-in self-test on an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a memory built-in self-test, including:

externally resetting a memory built-in self-test engine and a memory built-in self-test signature;

generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine; and

reading the generated memory built-in self-test signature.

34. The method of claim 33, wherein the execution of the memory built-in self-test includes:

initiating a plurality of components and signals in a memory built-in self-test engine and the memory built-in self-test signature register upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals in the memory built-in self-test domain; and

testing the flushed memory components.

35. The method of claim 33, wherein generating the memory built-in self-test signature includes storing the results in a memory built-in self-test signature register.

36. The method of claim 33, wherein performing the memory built-in self-test further includes at least one of:

performing at least one paranoid check; and

storing the results of the paranoid check in the memory built-in self-test signature register.

37. The method of claim 33, wherein performing the memory built-in self-test further includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done.

38. The method of claim 33, wherein externally resetting the memory built-in self-test engine includes

externally resetting a memory built-in self-test engine including:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine.

39. The method of claim 33, further comprising:

performing a logic built-in self-test; and

reading the results of the logic built-in self-test.

5/6/04